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2193

Attorney Docket No. 1538.1020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shigeo ORII

Application No.: 09/998,160

Group Art Unit: 2193

Filed: December 3, 2001

Examiner: Jason D. Mitchell

Confirmation No.: 6156

For: PARALLEL EFFICIENCY CALCULATING METHOD AND APPARATUS

COMMUNICATION SUBMITTING REFERENCES

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The patentee is submitting herewith a copy of the European Search Report and the prior art references cited therein for the above-referenced application as follows:

1. Vincenzo PIURI, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "Static Evaluation Of Concurrency Degree In Multitask Environments" INTERNATIONAL CONFERENCE ON COMPUTERS AND APPLICATIONS. BEIJING, JUNE 23 - 27, 1987, WASHINGTON, IEEE COMPUTER SOC. PRESS, US, vol. CONF. 2, June 1987 (1987-06), pages 674-681, XP000757331.
2. CROVELLA Mack E. ET AL; "Parallel Performance Prediction Using Lost Cycles Analysis" SUPERCOMPUTING '94., PROCEEDINGS WASHINGTON, DC, USA 14-18 NOV. 1994, LOS ALAMITOS, CA, USA IEEE COMPUT. SOC, 14 November 1994 (1994-11-14), pages 600-609, XP010100520 ISBN: 0-8186-6605-6
3. Xiaodong ZHANG et al: Latency Metric: An Experimental Method For Measuring And Evaluating Parallel Program And Architecture Scalability" JOURNAL OF PARALLEL AND DISTRIBUTED COMPUTING, ELSEVIER, AMSTERDAM, NL, vol. 22, no. 3, 1 September 1994 (1994-09-01), pages 392-410, XP000477422 ISSN: 0743-7315.
4. YAN Young et al.: "Software Support For Multiprocessor Latency Measurement And Evaluation" IEEE TRANSACTIONS ON SOFTWARE ENGINEERING, IEEE SERVICE CENTER, LOS ALAMITOS, CA, US, vol. 23, no. 1, January 1997 (1997-01), pages 4-16, XP000697644 ISSN: 0098-5589 Sections 3, 6.1, 6.4.1

It is requested that these be placed in the file of the subject application.

Respectfully submitted,

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